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EXAMINER	
PERILLA, JASON M	

ART UNIT	PAPER NUMBER
2638	

DATE MAILED: 08/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/882,512	KEAVENEY ET AL.	
	Examiner	Art Unit	
	Jason M. Perilla	2638	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 May 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *27-29* is/are allowed.

6)☒ Claim(s) *1-13,18,19 and 22-25* is/are rejected.

7)☒ Claim(s) *14-17,20,21 and 26* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 June 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-29 are pending in the instant application.

Response to Arguments/Amendments

2. In view of the amendments to the claims filed May 19, 2005, the claim objections set forth in the first office action dated December 19, 2005 are withdrawn.

3. In view of the amendments to the claims and the remarks, the rejections of claims 10 and 24 under 35 U.S.C. § 112, second paragraph, are withdrawn.

4. In view of the amendments to the claims and the arguments, the prior art rejections under 35 U.S.C. § 102(b) of claim 11 as being anticipated by Shurboff (US 6049233) is withdrawn and the rejections of claims 13, 20-24, 26, 27, and 29 under 35 U.S.C. § 102(b) as being anticipated by Iga et al (US 5459755) have been withdrawn.

5. The arguments against the prior art rejections under 35 U.S.C. § 103(a) including at least Shurboff have been fully considered, but they are not persuasive.

The Applicant contests that the admitted difference between the prior art reference Shurboff and the instant application, namely the switching of the reference signal and feedback signal inputs with respect to the first and second storage elements, is not obvious in view of the reasons set forth in the first office action. While the first office action sets forth that the difference may be considered a matter of design choice and provides no advantage as understood by one having ordinary skill in the art, the Applicant provides an advantage being that the change in the position of the delay (the change in the position of the delay element equates, alternatively, to a switching of the

reference and feedback inputs among the first and second storage elements) moves the activity of the frequency dividing element away from the charge pump activity.

While the Examiner does acknowledge that the stated advantage noted by the Applicant may provide an advantage compared with the disclosure of Shurboff, one skilled in the art may nonetheless arrive at the claimed invention for the premise set forth according to the Examiner. That is, the purpose of the phase locked loop of Shurboff (fig. 11) is to have a stable and accurate output (fig. 11, ref. 1112) according to a phase detector which has a linear output response. Therefore, a delay is added according to the invention of Shurboff. Because the position of the delay (or, alternatively the switching of the reference and feedback inputs) would have no impact as to the accuracy and stability of the output of the phase locked loop of Shurboff, the difference is appropriately considered a matter of design choice. As broadly as claimed, the difference between the disclosure of Shurboff and that of the instant application apparently provides no advantage because the result is the same. While the stated advantage according to the Applicant may result in reaching a stable and accurate output according to the advantage, it is not claimed, and, as broadly as claimed, the "lack of advantage" reasoning of the Examiner may still lead one to arrive at the claimed invention.

6. New art rejections are set forth below according to the newly found reference Humphreys (US 6002273).

Drawings

7. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the second stretching element coupled to the first stretching element of claim 25 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

8. Claims 1-26 and 29 are objected to because of the following informalities:

Regarding claim 1, in lines 15-16, "a delay element" should be replaced by –a delay--.

Regarding claim 7, in line 6, "a phase difference signal" should be replaced by –the phase difference signal--.

Regarding claim 11, in line 4, "controllable oscillator" should be replaced by –a controllable oscillator--.

Regarding claim 13, in lines 4-5, "second storage element" should be replaced by –second storage elements--.

Regarding claim 23, in line 1, "the delay" is lacking antecedent basis.

Regarding claim 24, in line 1, "the delay" is lacking antecedent basis.

Regarding claim 29, in lines 2-3, "a first and a second input" should be replaced by –a

Appropriate correction is required.

Claim Rejections - 35 USC § 112

9. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

10. Claim 25 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claim 25, the claim is indefinite because parent claim 13 claims that the stretching is measured in the output of the first storage device relative to the output of the second storage device although both the outputs of the first and second storage devices are claimed to be stretched in dependent claim 25. Therefore, one is unable to determine how the stretching of the first output should be measured against the second

output as claimed in claim 13 when both outputs are stretched (it is implied that they are stretched by the same amount) according to claim 25.

Claim Rejections - 35 USC § 102

11. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

12. Claims 1, 4-8, 11, and 12 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Humphreys (US 6002273).

Regarding claim 1, Humphreys discloses a phase detection apparatus (fig. 1, ref. 110) for generating a phase difference signal (fig. 1, ref. 111) for use in a phase lock loop (PLL) (fig. 1), the apparatus having a first input for a reference signal (fig. 2, ref. 106), and a second input for a loop feedback signal (fig. 1, ref. 136), the apparatus comprising: a) a first storage element (fig. 2, ref. 210) having a clock input (fig. 2, "FR" input), a reset input ("R") and an output (fig. 2, ref. 211), b) a second storage element (fig. 2, ref. 215) having a clock input (fig. 2, FV input), a reset input ("R") and an output (fig. 2, ref. 220), c) a logic element (fig. 2, ref. 235) for logically combining the outputs of the first and second storage elements, the logic element having inputs coupled to the outputs of the two storage elements and an output coupled to the reset input of the first storage element, d) a delay element (fig. 2, ref. 220) coupled to the output of the logic element, the delay element having an output coupled to the reset element of the second storage element, wherein the reference signal is input to the clock input of the first

storage element and the loop feedback signal is input to the clock input of the second storage element, the provision of the delay at the reset input of the second storage element effecting a delay of a trailing edge of the output of the second storage element relative to a trailing edge of the output of the first storage element (fig. 4).

Regarding claim 4, Humphreys discloses the limitations of claim 1 as applied above. Further, Humphreys discloses that the logic element comprises a logic AND gate (fig. 2, ref. 235).

Regarding claim 5, Humphreys discloses the limitations of claim 1 as applied above. Humphreys further discloses that the two storage elements (fig. 2, refs. 210 and 215) are flip flops.

Regarding claim 6, Humphreys discloses the limitations of claim 5 as applied above. Humphreys further discloses that the flip flops are D type flip flops and that the inputs of the flip flops are coupled to logic high (fig. 2).

Regarding claim 7, Humphreys discloses the limitations of claim 1 as applied above. Humphreys further discloses by figure 3 that the output of the first storage element (PUC) and the output of the second storage element (PDC) are coupled to a first current source (305) having an enable input (310) coupled to the output of the first storage element and a second current source (320) having an enable input (315) coupled to the output of the second storage element, the first and second current sources being coupled to form an output (111, "IOUT") for the phase difference signal.

Regarding claim 8, Humphreys discloses the limitations of claim 1 as applied above. Further, as broadly as claimed, the phase detector of Humphreys is a tri-state

phase frequency detector for at least the reasons that the phase detector of the instant application is a tri-state phase frequency detector because the phase detector of the instant application and that of Humphreys are identical in form and function.

Regarding claim 11, Humphreys discloses the limitations of the phase detection apparatus (e) as applied to claim 1 above. Further, Humphreys discloses a phase lock loop (fig. 1) apparatus having a reference signal input (F_R) and an oscillator output (fig. 1, ref. 121), the apparatus comprising: a) a filter element (fig. 1, ref. 115) having an input and an output, b) controllable oscillator device or VCO (fig. 1, ref. 120) having a control input coupled to the output of the filter element and an output adapted to produce the oscillator output, a frequency dividing element (fig. 1, ref. 135) having a first input coupled to the output of the oscillator output and an output for producing a feedback loop signal (fig. 1, ref. F_V), and d) a charge pump having two inputs coupled to the outputs of the storage elements and an output adapted to provide a phase difference signal as an input to the filter element as applied to claim 7 above.

Regarding claim 12, Humphreys discloses the limitations of claim 11 as applied above. Further, Humphreys discloses that the frequency dividing element comprises an interpolator or fractional-N modulator (fig. 1, refs. 130 and 135).

13. Claims 13, 18, 19 and 22 are rejected under 35 U.S.C. 102(b) as being anticipated by Aaron et al (US 3697690; hereafter "Aaron").

Regarding claim 13, Aaron discloses a phase detection apparatus by figure 3 comprising, according to figure 5, a first storage element (50) having a clock input (S), a reset input (R) and an output (I), a second storage element (50) having a clock input

(S), a reset input (R) and an output (I), a logic element (56) for logically combining the outputs of the first and second storage elements, the logic element having two inputs coupled to the outputs of the two storage elements and an output coupled to the reset input of the first storage element and the reset input of the second storage element (fig. 3; col. 6, lines 58-61), and a stretching element (54) for effecting a stretching of the trailing edge of the output of one of the first and second storage elements relative to the other storage element. Aaron discloses that the dead band phase detector (fig. 5) is used in the phase detection apparatus (fig. 3). Further, the reset (R) inputs of the phase detector are divided from the output of the logic element (fig. 5, ref. 56). Therefore, the output of the logic element is coupled to the reset inputs of the first and second storage elements.

Regarding claim 18, Aaron discloses the limitations of claim 13 as applied above. Further, Aaron discloses that the stretching element (fig. 5, ref. 54) stretches the trailing edge output of the first storage element relative to a trailing edge output of the second storage element. That is, the pulse stretcher 54 affects the output of the first storage element (fig. 5, ref. 50) and not the second storage element (fig. 5, ref. 51).

Regarding claim 19, Aaron discloses the limitations of claim 13 as applied above. Further, Aaron discloses that the stretching element (fig. 5, ref. 55) stretches the trailing edge output of the second storage element relative to a trailing edge output of the first storage element. That is, the pulse stretcher 55 affects the output of the second storage element (fig. 5, ref. 50) and not the first storage element (fig. 5, ref. 51).

Regarding claim 22, Aaron discloses the limitations of claim 13 as applied above. Further, as broadly as claimed, the phase detector of Aaron is a tri-state phase frequency detector for at least the reasons that the phase detector of the instant application is a tri-state phase frequency detector because the phase detector of the instant application and that of Aaron are substantially identical in form and function.

Claim Rejections - 35 USC § 103

14. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

15. Claims 1-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shurboff (US 6049233 – previously cited).

Regarding claim 1, Shurboff discloses by figure 1 a phase detection apparatus (abstract) for generating a phase difference signal for use in a phase lock loop (PLL), the apparatus having a first input (132) for a reference signal, and a second input (122) for a loop feedback signal, the apparatus comprising: a) a first storage element (104) having a clock input (132), a reset input (134) and an output (136), b) a second storage element (102) having a clock input (122), a reset input (124) and an output (126), c) a logic element (118) for logically combining the outputs of the first and second storage elements, the logic element having inputs coupled to the outputs of the two storage elements and an output coupled to the reset input of the first storage element, d) a delay element (110) coupled to the output of the logic element (118), the delay element

having an output coupled to the reset element (124) of the second storage element (102), the provision of the delay element (110) at the reset input of the second storage element effecting a delay of a trailing edge of the output of the second storage element relative to a trailing edge of the output of the first storage element. It is inherent that the delay of the reset of the second storage register will effect a delay of a trailing edge of the output of the second storage element. In the particular disclosure of Shurboff, the reference signal (F_R) is applied to the input clock of the second storage element rather than that of the first storage element as claimed, and likewise, the feedback signal (F_V) is applied to the clock input of the first storage element rather than that of the second storage element as claimed. However, as understood by one having ordinary skill in the art, the difference between the disclosure of Shurboff and that of the instant invention are such that the difference could reasonably be considered a matter of design choice. The Applicant has not disclosed that the particular input of the reference and feedback signals to storage elements provides an advantage, is used for a particular purpose, or solves a stated problem. One of ordinary skill in the art, furthermore, would have expected Applicant's invention to perform equally well with the disclosed reference and feedback connections as disclosed by Shurboff because the nature of the phase detector is simply to ascertain any difference between two input phases. Therefore, it would have been obvious to one having ordinary skill in the art at the time which the invention was made to apply the reference input to the first storage input and the feedback signal to the second storage element because in the case of inputs to a phase detector the order of the inputs is not consequential to the function of the phase detector

as reasonably understood by one having ordinary skill in the art and it would be considered a matter of design choice.

Regarding claim 2, Shurboff discloses the limitations of claim 1 as applied above. Shurboff further discloses by figure 1 a second delay element (114) with an input coupled to the output of the logic element (118), the second delay element having an output (152) coupled to the reset element of the first storage element (134) and wherein the delay introduced by the second delay element to the first storage element is less than the delay introduced by the first delay element to the second storage element. Because the delay of the second delay element (114) is the only delay applied to the reset of the first storage device and both the delays of the first and second delay elements (110 and 114, respectively) are applied to the reset of the second storage element, the delay introduced by the second delay element to the first storage element is less than the delay introduced by the first delay element to the second storage element because the delays are additive.

Regarding claim 3, Shurboff discloses the limitations of claim 1 as applied above. Shurboff further discloses by figure 1 a second delay element (114) coupled between the logic element (118) and the first delay element (110), the output of the second delay element being coupled to the reset element of the first storage element and the input of the first delay element.

Regarding claim 4, Shurboff discloses the limitations of claim 1 as applied above. Shurboff further discloses that the logic element comprises a logic AND gate (fig. 1, ref. 118; col. 2, lines 12-20)).

Regarding claim 5, Shurboff discloses the limitations of claim 1 as applied above. Shurboff further discloses that the two storage elements (fig. 1, refs. 102 and 104) are flip flops (col. 2, lines 12-20).

Regarding claim 6, Shurboff discloses the limitations of claim 5 as applied above. Shurboff further discloses that the flip flops are D type flip flops and that the inputs of the flip flops are coupled to logic high (col. 2, lines 12-30).

Regarding claim 7, Shurboff discloses the limitations of claim 1 as applied above. Shurboff further discloses by figure 1 that the output of the first storage element (136) and the output of the second storage element (126) are coupled to a first current source (108) (col. 2, lines 30-45) having an enable input (144) coupled to the output of the first storage element and a second current source (106) having an enable input (140) coupled to the output of the second storage element, the first and second current sources being coupled to form an output (142, "CURRENT OUTPUT) for a phase difference signal.

Regarding claim 8, Shurboff discloses the limitations of claim 1 as applied above. Further, as broadly as claimed, the phase detector of Shurboff is a tri-state phase frequency detector for at least the reasons that the phase detector of the instant application is a tri-state phase frequency detector because the phase detector of the instant application and that of Shurboff are substantially identical in form and function.

16. Claims 9-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shurboff in view of Gailbreath, Jr. (US 4795985; hereafter "Gailbreath" – previously cited).

Regarding claim 9, Shurboff discloses the limitations of claim 1 as applied above. Although Shurboff discloses that the delay element creates a relative delay, Shurboff does not explicitly disclose that the relative delay is programmable. However, Gailbreath teaches a phase locked loop using a programmable delay line (fig. 1, ref. 12; abstract). Gailbreath teaches that the programmable delay line provides up to 66ns of delay in 2ns steps. Gailbreath further teaches that the programmable delay may be programmed to delay in the direction that minimizes the phase error between the data transitions and reference clock. (col. 1. line 60 – col. 2, line 8). In the case of the invention of Shurboff, the delay lines could be of the programmable type to appropriately accommodate for minimizing phase differences and properly adjusting the linearity of the output characteristic of the charge pump. One skilled in the art would properly understand the advantages of a programmable delay line being that the system could be more appropriately and efficiently tailored. Therefore, it would have been obvious to one having ordinary skill in the art at the time which the invention was made to utilize programmable delay lines as taught by Gailbreath as the delay elements of Shurboff because the delay lines could be easily tailored to minimize phase differences and assist in creating a linear output characteristic of the charge pump.

Regarding claim 10, Shurboff in view of Gailbreath disclose the limitations of claim 9 as applied above. Further, because the purpose of the delay is to remove the non-linear region of operation from the phase detection apparatus, it is obvious that the delay would be at least as long as the time difference between the maximum deviation of the phase difference of the second element's clock input. As understood by one

having ordinary skill in the art, at the time of phase lock, the delay must be at least great enough to overcome the region of non-linearity. Therefore, it would have been obvious to one having ordinary skill in the art at the time which the invention was made to utilize a delay at least as great as the time difference between the maximum deviation in phase of the clock input to the second storage element because it would allow the region of non-linearity to be overcome even during a period of phase lock.

17. Claim 24 is rejected under 35 U.S.C. 103(a) as being unpatentable over Aaron.

Regarding claim 24, Aaron discloses the limitations of claim 23 as applied above. Further, because the purpose of the delay is to remove the non-linear region of operation from the phase detection apparatus (col. 2, lines 35-51), it is obvious that the delay would be at least as long as the time difference between the maximum deviation of the phase difference of the second element's clock input. As understood by one having ordinary skill in the art, at the time of phase lock, the delay must be at least great enough to overcome the region of non-linearity. Therefore, it would have been obvious to one having ordinary skill in the art at the time which the invention was made to utilize a delay at least as great as the time difference between the maximum deviation in phase of the clock input to the second storage element because it would allow the region of non-linearity to be overcome even during a period of phase lock.

18. Claim 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over Aaron in view of Gailbreath, Jr. (US 4795985; hereafter "Gailbreath" – previously cited).

Regarding claim 23, Aaron discloses the limitations of claim 13 as applied above. Aaron discloses that the stretching element stretches the output of the trailing edge of

the first storage element, but does not explicitly disclose that the stretch in the trailing edge is programmable. However, Gailbreath teaches a programmable delay utilized in a phase locked loop wherein the programmable delay can be programmed in 2ns steps for accuracy and flexibility (col. 1, line 65 – col. 2, line 5). Therefore, it would have been obvious to one having ordinary skill in the art at the time which the invention was made to utilize a programmable stretching element or delay as taught by Gailbreath in the apparatus of Aaron because it could be advantageously be used to add accuracy and flexibility to the circuit.

Allowable Subject Matter

19. Indication of allowable subject matter is made regarding claims 27-29.

20. The following is a statement of reasons for the indication of allowable subject matter:

Claims 27-29 are indicated to contain allowable subject matter because the prior art of record does not disclose or obviate all of the claimed features of independent claim 27. Specifically, although the prior art reference Aaron discloses the features of claim 13, Aaron does not disclose all of the claimed features of claim 27 because it does not disclose (or combine appropriately with) a charge pump having two inputs and an output.

21. Claims 14-17, 20, 21, and 26 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

22. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jason M. Perilla whose telephone number is (571) 272-3055. The examiner can normally be reached on M-F 8-5 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Vanderpuye Kenneth can be reached on (571) 272-3078. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jason M. Perilla
July 22, 2005

jmp

CHIEH M. FAN
PRIMARY EXAMINER